In The Specification

Please replace paragraph 005 with the following re-written paragraph:

005 Solder bumps may be formed by, for example, vapor deposition of solder material over layers of under bump metallization (UBM) formed on the chip bonding pad. In another method, the layers of solder material may be deposited by electrodeposition onto [[a]] seed layer material deposited over UBM layers formed on the chip bonding pad. In yet another method, solder bumps may be formed by a solder-paste screen printing method using a mask (stencil) to guide the placement of the solder-paste. Typically, after deposition of the solder materials, for example, in layers or as a homogeneous mixture, the solder bump (ball) is formed after removing a photoresist mask defining the solder material location by heating the solder material to [[a]] melting, ~~point~~ where according to a reflow process, a solder ball is formed with the aid of surface tension. Alternatively, a solder bump (column) may be formed within a permanent mask made of photoresist or some other organic resinous material defining the solder bump area over the chip bonding pad.

Please replace paragraph 008 with the following re-written paragraph:

008 One problem with the prior art in forming a solder bump relates to the thermal degradation of the photoresist layer following a first reflow process carried out for example, on stenciled solder paste prior to removing the photoresist layer (stencil) by wet chemical stripping. In many cases, especially with high lead alloys, temperatures greater than 350 °C may be required for proper reflow treatment of the solder paste. At these temperatures, typical photoresist materials thermally degrade and adhere to the semiconductor process wafer surface, for example, to the passivation layer. After degradation, the photoresist is difficult to remove by conventional wet stripping processes and frequently leaves a residue over the wafer surface. As a result, the photoresist residue may adversely affect subsequent semiconductor wafer processing steps. For example, the photoresist residue may adversely affect the second reflow process to form the solder ball, for example interfering with proper wetting of the UBM layer.

Please replace paragraph 0026 with the following re-written paragraph:

0026 Figure 3A-3C are cross-sectional side view representations of an exemplary process according to the present invention for forming a solder bump over the protective layer according to the present invention at selected stages in a manufacturing process.

Please replace paragraph 0027 with the following re-written paragraph:

0027 The method according to the present invention is more clearly described by referring to Figure 2A which is a representative cross-sectional side view ~~representation~~ of a stage in a manufacturing process for creating a solder bump bonded to a UBM layer overlying a chip bonding pad. For example, with reference to Figure 2A, the process of creating the solder bumps begins after chip bonding pad 20, for example Cu or Al, typically formed by vapor deposition, has been deposited on the surface of the substrate 21, for example an underlying layer forming a portion of a semiconductor device and forming a surface

of a semiconductor process wafer. After the chip bonding pad 20 is formed, a passivation layer 22 of, for example, silicon nitride (SiN), or silicon dioxide (SiO_2) is formed over the semiconductor device surface excluding a portion overlying the chip bonding pad 20. Typically, at least one under bump metallization (UBM) layer, e.g., 24A of from about 500 Angstroms to about 5000 Angstroms in thickness is then deposited, for example by physical vapor deposition, over the semiconductor process wafer surface including chip bonding pad 20.

Please replace paragraph 0028 with the following re-written paragraph:

0028 According to the method of the present invention, following deposition of the UBM layer 24A, more UBM layers may be optionally deposited (not shown). In an exemplary embodiment for example, the UBM layer 24A is a lowermost UBM layer of ~~for example~~ titanium followed by a copper layer (not shown) and an uppermost contact layer (not shown), for example nickel, for forming a solder bump thereover. In the exemplary embodiment shown in Figure 2A, the UBM layer 24A also forms the contact layer. A first layer of photoresist 24B for masking the at least

one UBM layer is then deposited and patterned and developed by conventional photolithographic processes to leave photoresist layer 24B forming an etching mask overlying the chip bonding pad 20 area including UBM layer 24A as shown in Figure 2B. The at least one UBM layer 24A is then etched according to a conventional reactive ion etching (RIE) process to remove the portion of UBM layer 24A area not covered by photoresist layer [[1]] 24B to reveal the passivation layer 22, for example, surrounding the chip bonding pad 20 as shown in Figure 2C.

Please replace paragraph 0030 with the following re-written paragraph:

0030 While a resinous organic material that has a thermal stability at temperatures greater than about 350°C is preferable, especially where high lead solder pastes are used which require reflow temperatures of greater than about 300°C, it will be appreciated that an organic resinous material that has thermal stability including a glass transition temperature (Tg) greater than about a thermal treatment temperature (reflow temperature) such that thermal degradation is avoided at the reflow temperature may be advantageously used according to the present invention. For example, if the glass transition temperature (Tg)

of the resinous organic material is about greater than (equal to or greater than) a reflow temperature (thermal treatment temperature), such a resinous organic material may be advantageously used according to the present invention to form protective layer 24C.

Please replace paragraph 0034 with the following re-written paragraph:

0034 Following the first reflow process, the photoresist layer 26 as well as the remaining underlying protective layer 24C [[is]] are removed according to a conventional wet chemical stripping procedure to leave the solder column 28A as shown in Figure 3B.

Please replace paragraph 0035 with the following re-written paragraph:

0035 According to the present invention, removal of the photoresist layer 16 and the underlying protective layer 24C results in a semiconductor process wafer surface including, for example, passivation layer 22 surface free of photoresist residue. As such, the subsequent second reflow process[[es]] to

form solder ball 28B as shown in Figure 3C [[are]] is accomplished without adverse affect from residual photoresist, [[and]] while ensuring that subsequent semiconductor packaging steps likewise proceed without adverse consequences from residual photoresist remaining on the process wafer surface, thereby increasing a throughput and semiconductor wafer package yield.